Appl. No.:   09/727,032
Amdt. dat d September 25, 2003
Reply to Office action of July 8, 2003

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (Currently amended) A computer system, comprising:

a computer bus coupling together a plurality of bus devices, wherein each of said plurality of bus devices includes a queue in which pending operations are stored while the bus device awaits access to the computer bus;

a bus arbiter coupled to the computer bus, said bus arbiter receiving requests from said plurality of bus devices to obtain access to the computer bus and indicating a number of operations pending in the queue of the bus device;

wherein said bus arbiter resolves conflicting requests from said bus devices based on the number of operations pending in the queue of the bus devices requesting bus accessthe workload of the bus devices that request access to the computer bus.

2.   (Cancelled).

3.   (Cancelled).

4.   (Currently amended) The system of claim 1[[3]], wherein each of said plurality of bus devices also asserts a signal to said bus arbiter indicating the number of operations pending in the queue.

5.   (Currently amended) The system of claim 1[[4]], wherein said bus arbiter compares the signals indicating the number of operations pending in the queue from any bus device[[s]] requesting access to the computer bus, and awards access to the computer busto the bus device with the most operations pending in its associated queue.

Appl. No.:   09/727,032
Amdt. dated Septemb r 25, 2003
Reply to Office action of July 8, 2003

6.   (Original) The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on a predetermined priority value assigned to each bus device.

7.   (Currently amended) The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on ~~the length of time since each~~ which device was last granted access ~~to the computer bus~~.

8.   (Original) The system of claim 5, wherein the signal indicating the number of operations pending in the queue comprises a multi-bit signal.

9.   (Original) The system of claim 8, wherein the multi-bit signal comprises n bits, with 2^n = number of entries in the queue of each device.

10.   (Currently amended) The system of claim 1[[3]], wherein the bus device access request indicates the number of operations pending in the queue of the bus device through a combination of specific numbers and at least one ~~each of said plurality of bus devices asserts a signal to said bus arbiter indicating a~~ range ~~value~~of operations pending in the queue.

11.   (Currently amended) A computer system, comprising:
        a bus;
        a plurality of bus devices, each of which couples to said bus, and each of which is capable of running cycles on said bus, and each of said bus devices includes a queue in which pending operations are stored while the bus device awaits access to the bus;
        a bus arbiter coupled to the bus, said bus arbiter receiving request signals from said plurality of bus devices that are seeking to run a cycle on said bus;
        wherein any of said devices that include one or more operations in its queue transmits ~~[[a]]~~ the request signal to said bus arbiter requesting access to

said bus and indicating a the number of operations pending in its associated queue; and wherein said bus arbiter resolves conflicting requests from said bus devices based on the number of operations pending in the queues of the requesting devices.

12.   (Currently amended) The system of claim 11, wherein each of said plurality of bus devices is capable of running bus cycles on said bus as a master device, and wherein said signal requesting access to said bus is a request for ownership of said bus.

13.   (Currently amended) The system of claim 11, wherein the request signal comprises a sideband signal between the bus devices and the bus arbiter with operations pending in a queue transmits a request signal indicating a request for access to said bus, and a workload signal indicating the number of operations pending in the queue.

14.   (Currently amended) The system of claim 13, wherein the queue associated with each bus device has a queue with the same number of entries.

15.   (Original) The system of claim 13, wherein at least two of said bus devices have queues with a different number of entries.

16.   (Currently amended) A method of resolving conflicting bus access requests in a computer bus, comprising the acts of:
       determining if more than one bus device has requested access to the computer bus;
       determining the workload associated with each bus device requesting access to the computer bus; and
       granting access to the bus device that has the greatest workload.

Appl. No.:   09/727,032
Amdt. dated September 25, 2003
Reply to Office action of July 8, 2003

17.   (Original) The method of claim 16, wherein the act of determining if more than one bus device has requested access includes monitoring for a request signal from each of the bus devices capable of initiating cycles on the computer bus.

18.   (Currently amended) The method of claim 16, wherein the act of determining the workload associated with each bus device includes receiving a signal from each device indicating a the-number of operations awaiting execution in that device.

19.   (Original) The method of claim 18, wherein the number of operations awaiting execution is determined based on the number of operations pending in a queue in that device.

20.   (Currently amended) The system of claim 16, further comprising an the act of breaking any ties between devices with equal workloads based on other priority criteria.